## 2022 ECP Community BOF Days

## OpenMP Roadmap for Accelerators Across DOE Pre-Exascale/Exascale Machines

Approved for public release

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Wednesday, May 11, 2022 11:00 AM – 12:30 PM ET

Joe Zerr (LANL)

Carlo Bertolli (AMD)

Ron Lieberman (AMD)

Greg Rodgers (AMD)

Office of

Science

Jeff Sandoval (HPE)



## **SPEAKERS**

- JaeHyuk Kwack (ANL) Introduction and moderator of vendors talks
- Kalyan Kumaran (ANL) Moderator of panel discussion
- Johannes Doerfert (ANL) Representative of LLVM and panelist
- Carlo Bertolli (AMD) Representative of AMD and panelist
- Tobias Burnus (GNU, Siemens) Representative of GNU and panelist
- Deepak Eachempati (HPE) Representative of HPE and panelist
- Xinmin Tian (Intel) Representative of Intel and panelist
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- Saiyed Islam (AMD)
- Ron Lieberman (AMD)
- Greg Rodgers (AMD)
- Jeff Sandoval (HPE)
- Barbara Chapman (HPE)
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## **MOTIVATION FOR THIS BOF**

- The current HPC environment is diverse and complex
  - Variety of hardware and multiple vendors providing their own programming interfaces and runtimes
- Critical for application developers to consider portable (and even better performance portable) solutions which can target different platforms across vendors
  - OpenMP is an open standard supported by nearly every vendor, and a promising solution
- Goals
  - Present vendors' OpenMP roadmap for DoE pre-exascale/exascale systems
  - Discuss performance and evaluation, interoperability, feature support and implementation details, and community support
  - Give advice to application developers about what works well in implementations (both now and in the future)





## MULTIPLE COMPILERS WILL SUPPORT A COMMON SETAs of 5/11/2022OF OPENMP DIRECTIVES ON GPUS (NON-EXHAUSTIVE LIST) (1/2)

✓ : yes
 (✓): yes with caveats
 X : no

	LLVM/Clang	AMD	HPE/Cray	Intel	NVIDIA	GNU (GCC 12)
	-		2 (teams, parallel or		NVIDIA	
Levels of parallelism	2 now, 3 under development	2 (teams, parallel)	simd)	3 (teams, parallel, simd)	2 (teams, parallel)	3 (teams, parallel, simd)
OpenMP directive						
target	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$
declare target	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$
map	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	√ (OMP 5.0)
target data	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$
target enter/exit data	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$
target update	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$
teams	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$
distribute	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$
parallel	$\checkmark$	$\checkmark$	$\checkmark$ (may be inactive)	$\checkmark$	$\checkmark$	$\checkmark$
for/do	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$
reduction	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$
simd	$\checkmark$ , GPU under development	√ (on host)	$\checkmark$	$\checkmark$	√ (ignored)	$\checkmark$
atomic	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	√ (OMP 5.1 ext)
critical	(√)	$\checkmark$	$\checkmark$	$\checkmark$	X	$\checkmark$
sections	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	X	$\checkmark$
master	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$
single	(√)	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$
barrier	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$
loop directive	eventually	√(recognize syntax)	√ (Fortran only)	$\checkmark$	$\checkmark$	$\checkmark$
collapse of a perfectly nested loop	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$
collapse of an imperfectly nested loop	$\checkmark$	√ (c/c++)	$\checkmark$	X	X	X (GCC13/OG12)
collapse of a non-rectangular nested loop	$\checkmark$	√ (c/c++)	$\checkmark$	×	X	C/C++: √ / F90: X (F90: GCC13/OG11)
loop transformation with tile	$\checkmark$	$\checkmark$	$\sqrt{(C/C++ only)}$	$\checkmark$	X	X (GCC13/OG12)
loop transformation with unroll	$\checkmark$	$\checkmark$	$\sqrt{(C/C++ only)}$	$\checkmark$	X	X (GCC13/OG12)
array reduction	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	√/ F90 array sections: 🗙
scan	eventually	√(recognize syntax)	X	X (WIP)	X	$\checkmark$

## MULTIPLE COMPILERS WILL SUPPORT A COMMON SET As of 5/11/2022 OF OPENMP DIRECTIVES ON GPUS (NON-EXHAUSTIVE LIST) (2/2)

√ : yes
(√): yes with caveats
X : no

	LLVM/Clang	AMD	HPE/Cray	Intel	NVIDIA	GNU (GCC 12)
requires unified shared memory	∠,olarig	$\checkmark$	√ (some platforms)	√	X (unnecessary)	X (WIP for nyptx)
requires dynamic_allocators	(√)	×	× (some platornis)	$\checkmark$	X (unnecessary)	(X) (GCC13/OG12)
declare reduction	$\checkmark$	$\checkmark$	$\sqrt{(C/C++ only)}$	$\checkmark$	×	$\checkmark$
declare mapper	$\checkmark$	$\checkmark$	$\sqrt{(C/C++ only)}$	$\checkmark$	X	X (GCC13/OG12)
metadirective	$\checkmark$	√(c/c++)	$(\checkmark)$ (limited, OMP 5.0 only)	X (WIP)	partial	X (GCC13/OG11)
declare variant	$\checkmark$	$\checkmark$	$(\checkmark)$ (limited, OMP 5.0 only)	$\checkmark$	partial	$\checkmark$
"target nowait" supporting asynchronous execution	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$(\checkmark)$ (sync w/ in_reduction)
"target depend" supporting fine-grained dependencies	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	X	$\checkmark$
"target device" supporting multiple non-host devices per process	$\checkmark$	$\checkmark$	X	$\checkmark$	$\checkmark$	$\checkmark$
use_device_addr	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	√ (+ has)
detachable tasks: "detach" clause and "omp_fulfill_event" runtime routine	(√)	$\checkmark$	$\checkmark$	X	X	$\checkmark$
Memory management APIs						
allocate directive for allocating variables in managed memory via allocator	(√)	$\checkmark$	√ (extension)	$\checkmark$	X	X (GCC13/OG11)
allocate clause for allocating privatized variables in managed memory via allocator	(√)	X	(extension)	$\checkmark$	X	$(\checkmark)$
APIs for allocating/freeing memory via allocator	$\checkmark$	<ul> <li>✓ (limited support on device with predefined allocators)</li> </ul>		$\checkmark$	×	$\checkmark$
APIs for defining new allocators with custom traits (e.g. pinned memory)	$\checkmark$	$\checkmark$ (only pinned)	$\checkmark$	$\checkmark$	X	$\checkmark$
Interop objects/directive and APIs	$\checkmark$	X	X	$\checkmark$	X	X
C++ attribute syntax	eventually	$\checkmark$	X	🗙 (WIP)	X	$\checkmark$
Orphaned parallel regions (any limitations? e.g. serialized)	No limitations	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$ , parallel but slow	$\checkmark$
Creating C++ objects containing virtual functions inside target regions (GPU)	$\checkmark$	X	$\checkmark$	X (WIP)	X	$(\checkmark)$ (if vtable+ methods emit.)
Mapping C++ objects containing virtual functions from host to the GPU	eventually	X	X	X (WIP)	X	$(\checkmark)$ (no virt. calls)
printf/print support in a target region (GPU)	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	√/ F90 on nvptx: X (GCC13/OG12)
Call CUDA/SYCL/HIP kernels in an OpenMP target region	$\checkmark$	×	X	$\checkmark$	CUDA works, but it depends on the details	(√) (may work)

## **OPENMP RESOURCES**

OpenMP website

- https://www.openmp.org
- OpenMP Validation and Verification
- https://crpl.cis.udel.edu/ompvvsollve/

OpenMP YouTube Channel

https://www.youtube.com/user/OpenMPARB/

**OpenMP Users Monthly Teleconferences** 

https://www.openmp.org/events/ecp-sollve-openmp-monthly-teleconference/

At 2022 ECP Annual Meeting:

- Early Experience of Application Developers with OpenMP Offloading
- Wed. May 4, 2022, 4:00 PM 6:00 PM (ET)
- Recording available at ECP Annual Meeting Page





## SCHEDULE AT THIS BOF

Topics	Minutes	Presenter or Moderator		
Introduction	3	JaeHyuk Kwack/ Colleen Bertoni		
Roadmap Presentations				
LLVM	7	Johannes Doerfert		
AMD	7	Carlo Bertolli		
GNU	7	Tobias Burnus		
HPE	7	Deepak Eachempati		
Intel	7	Xinmin Tian		
NVIDIA	7	Jeff Hammond		
Panel discussion <ul> <li>Preselected questions</li> <li>Questions/comments from audience (alternating)</li> </ul>	45	Kalyan Kumaran and other panelists		
Total time	90			





## **ROADMAP PRESENTATIONS**



U.S. DEPARTMENT OF ENERGY Argonne National Laboratory is a U.S. Department of Energy laboratory managed by UChicago Argonne, LLC.







LLVM/OpenMP in HPC A Brief Overview

## Building LLVM + OpenMP offloading

## Single command often suffices to configure:

cmake /src/llvm-project/llvm -DLLVM\_ENABLE\_PROJECTS='clang;lld' -DLLVM\_ENABLE\_RUNTIMES='openmp'
make -j

Screenshot me :)

Useful options include: CMAKE\_BUILD\_TYPE={Release,Asserts,...}
 LLVM\_ENABLE\_ASSERTIONS={ON,OFF}
 LLVM\_CCACHE\_BUILD={ON,OFF}
 -G Ninja

Various resources available online! Start here:

https://llvm.org/docs/GettingStarted.html
https://openmp.llvm.org/SupportAndFAQ.html

## LLVM/OpenMP Features

- Device-side LTO for OpenMP offload (and CUDA)
- OpenMP offloading to a remote process (or to remote GPUs)
- Host debugging on the OpenMP virtual GPU
- Mix CUDA device code and OpenMP offload code
- JIT compilation (and specialization) for OpenMP offload kernels
- Extraction of OpenMP kernels and isolated replay, tuning, etc. [WIP]

Screenshot me:)

- Portable wrapper for common libraries (Thrust, BLAS, ...) [WIP]

## OpenMP-Aware Optimizations

Automatic SPMDzation + shared memory usage (LLVM 13+)



Screenshot me :)

## OpenMP-Optimization Remarks & Assumptions

example.cpp:41:24: remark: Found thread data sharing on the GPU. Expect degraded performance due to data globalization. [OMP112] [-Rpass-missed=openmp-opt] double device\_function(float Arg) {

example.cpp:42:3: remark: Moving globalized variable to the stack. [OMP110] [-Rpass=openmp-opt] double Lcl;

 OpenMP-Opt emits remarks (above)
 The web provides explanations (right)
 Users add OpenMP assumptions, e.g., #pragma omp assume ext\_spmd\_amenable

# Moving globalized variable to the stack. [OMP110]

This optimization remark indicates that a globalized variable was moved back to thread-local stack memory on the device. This occurs when the optimization pass can determine that a globalized variable cannot possibly be shared between threads and globalization was ultimately unnecessary. Using stack memory is the best-case scenario for data globalization as the variable can now be stored in fast register files on the device. This optimization requires full visibility of each variable.

Globalization typically occurs when a pointer to a thread-local variable escapes the current scope. The compiler needs to be pessimistic and assume that the pointer could be shared between multiple threads according to the OpenMP standard. This is expensive on target offloading devices that do not allow threads to share data by default. Instead, this data must be moved to memory that can be shared, such as shared or global memory. This optimization moves the data back from shared or global memory to thread-local stack memory if the data is not actually shared between the threads.

#### Examples

A trivial example of globalization occurring can be seen with this example. The compiler sees that a pointer to the thread-local variable \* escapes the current scope and must globalize it even though it is not actually necessary. Fortunately, this optimization can undo this by looking at its usage.

void foo() {
 int x;
 use(&x);
}
int main() {
#pragma omp target parallel

void use(int \*x) { }

foo();

#include <complex>

icing\_complay\_\_\_std:.complay\_double\_.

\$ clang++ -fopenmp -fopenmp-targets=nvptx64 omp110.cpp -01 -Rpass=openmp-opt omp10.cpp:6:7: remark: Moving globalized variable to the stack. [OMP110] int x;

A less trivial example can be seen using C++'s complex numbers. In this case the overloaded arithmetic operators cause pointers to the complex numbers to escape the current scope, but they can again be removed once the usage is visible.

## Visit openmp.llvm.org for more!

https://openmp.llvm.org/remarks/OptimizationRemarks.html



## OpenMP offload Recommendations

- Use a recent (e.g., nightly) compiler version.
- Enable compilation remarks https://openmp.llvm.org/remarks/OptimizationRemarks.html

Screenshot me :)

- Use LIBOMPTARGET\_INFO(=16) to learn about the GPU execution https://openmp.llvm.org/design/Runtimes.html#libomptarget-info
- Use LIBOMPTARGET\_PROFILE for built in profiling support.
- Use LIBOMPTARGET\_DEBUG (and -fopenmp-target-debug) for runtime assertions and
  - other opt-in debug features https://openmp.llvm.org/design/Runtimes.html#debugging
- Consider assumptions for better performance:
  - LIBOMPTARGET\_MAP\_FORCE\_ATOMIC=false and -fopenmp-assume-no-thread-state
- Use device-side LTO -foffload-lto

# 

## OpenMP® Support of ROCm<sup>™</sup> v5.0 @ OpenMP RoadMap BoF

@2022 ECP Community BoF Day, 11<sup>th</sup> May 2022

- Carlo Bertolli & Saiyedul Islam

## **OffloadArch Library &** *offload-arch* **Tool**

- Tool (and LLVM<sup>™</sup> library) to query capabilities of the target runtime
  - Like, (arch name: gfx90a, or features like shared memory ECC turned on/off)
- Capabilities
  - Pre-decided characteristics of the target which require a dedicated image in a fat binary.
- libomptarget uses LLVM library interface to query the target system and extract a compatible image, if any.
- Works with multi-GPU systems as well
- Query a binary for list of image requirements

Option	Description
h	Print the help message.
а	Print values for all devices. Don't stop at first device found.
m	Print device code name (often found in pci.ids file).
n	Print numeric pci-id.
t	Print clang offload triple to use for the offload arch.
v	Verbose = -a -m -n -t For all devices, print codename, numeric value and triple
f <filenam e&gt;</filenam 	Print offload requirements including offload-arch for each compiled offload image built into an application binary file.
c	Print offload capabilities of the underlying system. This option is used by the language runtime to select an image when multiple images are available. A capability must exist for each requirement of the selected image.

## **Multi-architecture Compilation**

- Possible target configs:
  - 1. gfx906 and gfx906
  - 2. gfx908:xnack- and gfx908:xnack+
  - 3. (gfx906 and gfx908) or (sm\_70 and sm\_85)
  - 4. gfx906 and sm\_70

- Build a common binary which can run on one GPU at a time for any of the above configuration
- Build once, run anywhere!

- Generate a multi-image binary such that:
  - Each image is tagged and compiled for a specific target
    - create a ToolChain for each target in clang driver
  - Tags should be sufficient to uniquely describe its target
    - define "Requirements" of image
  - Images are packed in a (fat) binary
    - use clang-offload-wrapper
- Load the right image from the binary at the runtime, using mechanisms:
  - to identify characteristics of the current target (H/W + S/W configuration)
    - use OffloadArch library to identify "Capabilities" of current target
  - to test compatibility of current target with each image in the binary
    - modify libomptarget

```
clang -O2 -fopenmp-fopenmp-targets=amdgcn-amd-amdhsa,amdgcn-amd-amdhsa \
```

```
-Xopenmp-target=amdgcn-amd-amdhsa -march=gfx906:xnack- \
```

```
-Xopenmp-target=amdgcn-amd-amdhsa -march=gfx908:xnack+ \
```

helloworld.c -o helloworld

## **Unified Shared Memory**

- Modes:
  - Default Mode
  - USM Mode (maps are optional)
- Default mode → USM Mode (always portable)
- USM Mode → Default Mode (not necessarily)
- ROCm<sup>™</sup> AMDGPU Implementation USM Mode → maps give better performance
  - Maps  $\rightarrow$  Coarse grain memory
  - Coarse grain faster than fine grain
- Programs written for default mode will give best USM mode performance
- Maps are the way to incrementally improve performance of critical/hotspot kernels in USM mode

## Unified Shared Memory on ROCm<sup>™</sup> AMDGPU

```
#pragma omp requires unified_shared_memory
int main() {
  double *a = new double[n]:
  double *b = new double[n];
  #pragma omp target teams distribute parallel for map(tofrom: a[:n]) map(to: b[:n])
  for(int i = 0; i < n; i++)
    a[i] += b[i];
}
                If maps are used, pages used by a and b switch to coarse grain
```

• Still, <u>no</u> device memory allocation, nor memory copies

clang -fopenmp -fopenmp-targets=amdgcn-amd-amdhsa -Xopenmp-target=amdgcn-amd-amdhsa
-march=gfx90a helloworld.c -o helloworld

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# OpenMP in GCC Status & Tips

**Tobias Burnus** 

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## **GNU Compiler Collection (GCC) & OpenMP**

- Widely used & supported open-source software
  - contributing is simple & welcoming community
  - paid/unpaid contributors
  - Linux distros also pack offloading support (via optional packages)
- C17 (most of C2x), C++20 (most of C++23)
   Fortran: 2008 + coarray/interop TS (mostly), initial F2018
- OpenMP/OpenACC support in C, C++, Fortran
  - Full OpenMP 4.5, much of 5.0, some of 5.1
  - OpenACC 2.6
- Offloading to nvptx (Nvidia) + AMD GCN (Radeon)
- Annual major releases around late spring (~ end of April)
  - GCC 12: Released on May 6, 2022
  - GCC 11: Released April 2021, last 11.3 (April 2022)
  - $\rightarrow$  Linux distros use git branch directly, mainline also quite stable
  - $\rightarrow$  Also avail: OG12 (= devel/omp/gcc-12) SIEMENS' public branch



#### On Summit (OLCF/ORNL) [by compute time] Compiler Count By Family CY-2021

January - August, Total Count: ~3.4M



D. Bernholdt (ORNL) + T. Burnus, GCC, https://openmpcon.org/conf2021/program-archive/

## **OpenMP Now Supported & Implementation Status**

## GCC 11

- Non-rect loop nests, allocator routines, declare variant ext. (C/C++)
- Fortran: full OpenMP 4.5, order(concurrent), device\_type, memorderclauses for flush, lastprivate with conditional modifier, atomic construct and reduction clause 5.0 ext.
- GCN: gfx908 (MI100) support

## GCC 12

- OpenMP 5.1: C++ 11 attributes, masked/scope/error/nothing, atomic extensions, memory-allocation routines, strictly structured blocks
- OpenMP 5.0: affinity clause. Fortran: declare variant, depobj, mutexinoutset, iterator, defaultmap 5.0 ext., loop
- GCN: Debugging (ROCGDB), wavefronts per compute unit restrictions lifted, wavefront-workgroup tunings
- NVPTX: Updates related to sm\_xx target and PTX ISA

Mainline (GCC 13): Several OpenMP patches already pending

#### **Supported Releases**

#### GCC 12.1 (changes)

Status: 2022-04-28 (frozen for release). Serious regressions. All regressions.

#### GCC 11.3 (changes)

Status: 2022-04-21 (regression fixes & docs only). Serious regressions. All regressions.

#### GCC 10.3 (changes)

Status: 2021-04-08 (regression fixes & docs only). Serious regressions. All regressions.

#### GCC 9.4 (changes)

Status: 2021-06-01 (regression fixes & docs only). Serious regressions. All regressions.

Development: GCC 13.0 (release criteria, changes) Status: 2022-04-28 (general development). Serious regressions. All regressions.

#### **2 OpenMP Implementation Status**

• OpenMP 4.5:	Feature completion status to 4.5 specification
• OpenMP 5.0:	Feature completion status to 5.0 specification
• OpenMP 5.1:	Feature completion status to 5.1 specification

 $GCC \rightarrow 12$  Changes  $\rightarrow$  OpenMP or https://gcc.gnu.org/onlinedocs/libgomp/ Following OpenMP Spec, Appendix B

## **SIEMENS**

## Compiling

## **Enabling offloading**

- -fopenmp automatically enables offloading for omp target regions
- -fopenmp-simd only SIMD, no parallelization/lib dependency
- -foffload=[disable|default|nvptx-none,amdgcn-amdhsa,...]
   Disable offloading, use default (all avail), or only specified types (list)

## Argument passing to offload compiler

-foffload-options=-Im -foffload-options=nvptx-none=-latomic
 GCC <12: Use -foffload= instead (undocumented, has corner case)</li>

## Optimization

- -O0 (default), -O1/-O2/-O3, -Og, -Ofast ( $\rightarrow$  -ffast-math)
- -mveclibabi=[svml,acml,mass] vector math libs by Intel/AMD/IBM

## Diagnostic

 -fopt-info-... (-fopt-info-loops, -fopt-info-omp, -fopt-info-vec-missed, ...): Checking/debugging optimizations

-foffload-options=options
-foffload-options=target-triplet-list=options

With -foffload-options=options, GCC passes the specified options to the compilers for all enabled offloading targets. You can specify options that apply only to a specific target or targets by using the -foffload-options=target-list=options form. The target-list is a comma-separated list in the same format as for the -foffload= option.

Typical command lines are

-foffload-options=-lgfortran -foffload-options=-lm -foffload-options="-lgfortran -lm" -foffload-options=nvptx-none=-latomic -foffload-options=amdgcn-amdhsa=-march=gfx906 -foffload-options=-lm

(Since GCC 12) Manpage or https://gcc.gnu.org/onlinedocs/gcc/



## **Offload Targets**

## Nvidia GPUs (nvptx)

- GCC generates nvptx (generic code)
- JIT compiled by CUDA run-time library at startup (→ CUDA\_CACHE docu)
- -march=sm\_xx (GCC 12) / -misa=sm\_xx (alias + GCC < 12) sm\_30, sm\_35, (GCC 12:) sm\_53, sm\_70, sm\_75, sm\_80
- -march-map=sm\_xx: (GCC 12) maps sm\_xx to a supported sm\_xx (↑)
- <u>https://github.com/MentorEmbedded/fortran-cuda-interfaces</u> cublas, cublas\_v2, cublasxt, openacc\_cublas, cufft

#### AMD GCN

- GCN generates code for: fiji (GCN3, gfx803), gfx900/gfx906 (GCN5, VEGA 10/20), gfx908 (MI100)
  - Example: -fopenmp-options=-march=gfx908
- Offload debugging with GCC 12 and ROCGDB: <a href="https://linuxplumbersconf.org/event/11/contributions/997/">https://linuxplumbersconf.org/event/11/contributions/997/</a>



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## Hewlett Packard Enterprise

# HPE OPENMP COMPILER UPDATE

Deepak Eachempati CCE OpenMP Compiler Group

May 11, 2022

## HPE CRAY COMPILING ENVIRONMENT (CCE)

- Fortran compiler
  - Proprietary front end and optimizer; HPE-modified LLVM backend
  - Fortran 2018 support (including coarray teams)
- C and C++ compiler
  - HPE-modified closed-source build of Clang+LLVM complier
  - C11 and C++17 support
  - UPC support
- OpenMP Offloading support for NVIDIA/AMD GPUs
  - OpenMP 4.5 and partial 5.0/5.1
  - some differences between Fortran and C/C++ compilers in support
  - Other models available: OpenACC 2.0 (Fortran only), HIP (C++, AMD GPUs only)

## **CCE OPENMP SUPPORT**

- Uses proprietary OpenMP runtime libraries
- Supports cross-language and cross-vendor OpenMP interoperability
  - CCE's libcraymp behaves as drop-in replacement for Clang's libomp and GNU's libgomp
  - GNU OpenMP interface support is limited to OpenMP 3.1 constructs update planned for future release
- Implements HPE-optimized code generation for OpenMP offload regions
- OpenMP 5.0 and 5.1 in progress, implemented over several CCE releases
  - See release notes and intro\_openmp man page for full list of supported features
  - OpenMP 5.0 is near complete as of CCE 13.0 (Nov 2021)
  - OpenMP 5.1/5.2 support in progress for 2022-2023

## **CCE OPENMP 5.0 STATUS**

CCE 10.0 (May 202	0)
-------------------	----

#### CCE 11.0 (Nov 2020)

#### CCE 12.0 (Jun 2021)

conditional lastprivate (C/C++)

• iterator in depend (C/C++)

depobj for depend (C/C++)

simd nontemporal (C/C++)

Ivalue list items for depend

CCE 13.0 (Nov 2021)

declare variant (C/C++)

mapper (C/C++)

metadirectives (C/C++)

close modifier (Fortran)

mutexinoutset (Fortran)

extend defaultmap (Fortran)

taskloop cancellation (C/C++)

mutexinoutset (C/C++)

task reduction (C/C++)

task modifier (C/C++)

device\_type (Fortran)

• affinity clause

• simd if (C/C++)

scan (C/C++)

- OMP\_TARGET\_OFFLOAD
- reverse offload
- implicit declare target
- omp\_get\_device\_num
- OMP\_DISPLAY\_AFFINITY
- OMP\_AFFINITY\_FORMAT
- set/get affinity display
- display/capture affinity
- requires
- unified\_address
- unified\_shared\_memory
- atomic\_default\_mem\_order
- dynamic\_allocators
- reverse\_offload
- combined master constructs
- acq/rel memory ordering (Fortran)
- deprecate nested-var
- taskwait depend
- simd nontemporal (Fortran)
- Ivalue map/motion list items
- allow != in canonical loop
- close modifier (C/C++)
- extend defaultmap (C/C++)

- noncontig updatemap Fortran DVs
- map Fortran DVs
- host teams
- use\_device\_addr
- nested declare target
- allocator routines
- OMP\_ALLOCATOR
- allocate directive
- allocate clause
- order(concurrent)
- atomic hints
- default nonmonotonic
- imperfect loop collapse
- pause resources
- atomics in simd
- simd in simd
- detachable tasks
- omp\_control\_tool
- OMPT
- OMPD
- declare variant (Fortran)
- loop construct
- metadirectives (Fortran)
- pointer attach
- array shaping
- acq/rel memory ordering (C/C++)
- device\_type (C/C++)
- non-rectangular loop collapse (C/C++)

- .
  - task reduction (Fortran)
  - task modifier (Fortran)
  - target task reduction (Fortran)
  - simd if (Fortran)

#### **Future CCE Release**

- loop construct (C/C++)
- mapper (Fortran)
- iterator in depend (Fortran)
- non-rectangular loop collapse (Fortran)
- depobj for depend (Fortran)
- uses\_allocators
- concurrent maps
- taskloop cancellation (Fortran)
- scan (Fortran)
- target task reduction (C/C++)

Refer to CCE release notes or intro\_openmp man page for current implementation status

## 2021) CCE 14.0 (May 2022)

## **OPENMP CONSTRUCT MAPPING TO GPU**

NVIDIA	AMD	CCE Fortran OpenACC	CCE Fortran OpenMP	CCE C/C++ OpenMP	Clang C/C++ OpenMP
Threadblock	Work group	acc gang	omp teams	omp teams	omp teams
Warp	Wavefront	acc worker		omp parallel or	omp parallel
Thread	Work item	acc vector	omp simd	omp simd	

- Current best practice:
  - Use **teams** to express GPU threadblock/work group parallelism
  - Use **parallel for simd** to express GPU thread/work item parallelism
- Future direction:
  - Improve CCE support for **parallel** and **simd** in accelerator regions
  - Upstream Clang is expanding support for **simd** in accelerator regions

Long-term goal: let users express parallelism with any construct they think makes sense, and CCE will map to available hardware parallelism

## **ASYNC OFFLOAD CAPABILITIES**

- OpenMP offload **nowait** constructs map to independent GPU streams
  - **depend** clauses are handled with necessary stream synchronization
- Task "detach" support introduced in CCE 11.0 (Nov 2020)
- Cross-device dependences are not yet optimized well (overly conservative synchronization)
- Multi-threaded use of GPU is optimized as of CCE 13.0 (Nov 2021) relaxed locking strategy

# **THANK YOU**

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# Intel<sup>®</sup> Compilers Update

Xinmin Tian Intel Corporation ECP OpenMP Community RoadMap BoF'2022


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### Agenda

- OpenMP Standards Support in Intel<sup>®</sup> Compilers
- Unified Shared Memory (USM) allocators
- OpenMP and SYCL/DPC++ Composability
- Async Offloading
- OpenMP SIMD
- Fortran (IFX) Status Update

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### OpenMP Standards Support in Intel compilers

- OpenMP 4.0/4.5 offloading will not supported in ICC and IFORT for GPUs and will not be conformant to OpenMP 5.0/5.1.
- OpenMP 5.0/5.1/5.2 features are planned to be implemented in ICX and IFX by continuously leveraging Clang/LLVM community work.

Intel Compiler	Driver	Target*	OpenMP Support	OpenMP Offload Support	Included in oneAPI Toolkit	
Intel <sup>®</sup> C++ Compiler Classic (ICC)	icc	CPU	Yes	No	HPC, IoT	
Intal® and ADI DDC II (CIII Compiler (ICX)	dpcpp	CPU, GPU, FPGA	Yes	Yes	Base	
Intel <sup>®</sup> oneAPI DPC++/C++ Compiler (ICX)	ісх	CPU GPU	Yes	Yes	Base	
Intel <sup>®</sup> Fortran Compiler Classic (IFORT)	ifort	CPU	Yes	No	HPC	
Intel <sup>®</sup> Fortran Compiler (Beta) (IFX)	ifx	CPU, GPU	Yes	Yes	HPC	

### Use OpenMP Memory Allocator for USM

program reduction_example	val_ver = 0.0
use omp_lib	!\$omp target data map(tofrom: val_ver) map(to: a_x, b_x, c_x)
integer :: n = 32768	!\$omp target teams distribute parallel do reduction(+: val ver)
integer :: m = 2048	& collapse(2)
integer :: i, j	
double precision :: val = 0.0	do i = 1, n
double precision :: val_ver = 0.0	do j = 1, m
double precision, allocatable :: a_h(:), b_h(:), c_h(:)	val_ver = val_ver + a_x(i) * b_x(i) * c_x(i);
real*8 a_x(32768), b_x(32768), c_x(32768)	end do
	end do
<pre>!\$omp allocate allocator(omp_target_shared_mem_alloc) allocate(a h(n))</pre>	\$ somp end target teams distribute parallel do!
	!\$omp end target data
!\$omp allocate allocator(omp_target_shared_mem_alloc)	
allocate(b_h(n))	if(abs(int(val*1.0d+15) - int(val_ver*1.0d+15)) .lt. 1.0) then
	write(*,*) "Congratulations!! Correct Results"
!\$omp allocate allocator(omp_target_shared_mem_alloc)	write(*,*) " val[",
allocate(c_h(n))	& val, "]; val_ver[", val_ver, "]"
do i = 1, n	else
a_h(i) = dble(i);	write(*,*) "Incorrect Result", " val[",
b_h(i) = 0.2;	& val, "]; val_ver[", val_ver, "]"
c_h(i) = 0.3;	endif
a_x(i) = dble(i);	
b_x(i) = 0.2;	deallocate(a_h)
c_x(i) = 0.3;	
end do	deallocate(b_h)
	deallocate(c_h)
! Reduction on val is done in C implementation below	end program
call red 02(a h, b h, c h, n, m, val)	

### OpenMP and SYCL/DPC++ Composability

- Several codes might need a smooth transition to/from OMP offload and DPC++
- Question coming from many customers
- A very simple test just to understand how compilation and execution works

### Offloading 2 Different Kernels

- Simple main.cpp
- We are creating 2 OMP tasks each one sending a kernel
- The first kernel is OMP
- The second kernel is DPC++

#pragma omp parallel sections shared(size)

//OMP target section
#pragma omp section

run\_omp(Aomp, Bomp, Comp, size);

//DPCPP section
#pragma omp section

run\_dpcpp(Adpcpp, Bdpcpp, Cdpcpp, size);

### Asynchronous Offloading

```
#include <stdio.h>
                                                        Added compiler support of enabling free agent helper
#include <omp.h>
                                                        thread running concurrently with the initial thread
int main() {
  int ret = 0;
                                                        Leveraged community free agent helper thread
#pragma omp target map(ret) nowait
                                                        support
    for (int i = 0; i < 1000; i++)</pre>
      for (int j = 0; j < 1000; j++)</pre>
        ret--;
    if (ret <= 0)
      ret = 1;
    printf("Device ret = %d\n", ret);
  printf("Before explicit offload sync: ret = %d\n", ret);
#pragma omp taskwait
  printf("After explicit offload sync: ret = %d\n", ret);
  return 0;
xtian@scsel-cfl-12:$ icpx -fiopenmp -fopenmp-targets=spir64 target nowait.cpp -o run.x
xtian@scsel-cfl-12:$ ./run.x
Before explicit offload sync: ret = 0
Device ret = 1
After explicit offload sync: ret = 1
```

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### OpenMP SIMD for GPUs

```
#pragma omp target enter data map( alloc:a[0:TOTAL_SIZE] )
#pragma omp target enter data map( alloc:b[0:TOTAL_SIZE] )
#pragma omp target update to(a[0:TOTAL_SIZE])
#pragma omp target update to(b[0:TOTAL_SIZE])
#pragma omp target update to(b[0:TOTAL_SIZE])
const int no_max_rep = 400;
double time = omp_get_wtime();
for ( int irep = 0; irep < no_max_rep; ++irep ) {
    #pragma omp target teams distribute parallel for
    for ( int isimd = 0; isimd < TOTAL_SIZE; isimd += SIMD_SIZE<>2) {
    #pragma omp simd simdlen(32)
```

```
for (int ilane = 0; ilane < SIMD_SIZE<<2; ++ilane) {
    const int index = isimd + ilane;
    c[index] = a[index] + b[index];</pre>
```

```
time = omp_get_wtime() - time;
time = time/no max rep;
```

```
#pragma omp target exit data map( release:a[0:TOTAL_SIZE] )
#pragma omp target exit data map( release:b[0:TOTAL_SIZE] )
#pragma omp target exit data map( release:c[0:TOTAL_SIZE] )
```

### Fortran (IFX) Compiler Status Update

- F2003 complete (PDT's now implemented)
- F2008 complete except coarrays (F2008 in Q3, F2018 in Q4)
- F2018 development (IEEE compares, DIM opt arg in intrinsics)
- Fortran extension VAX structs/unions implemented
- Complete IFX OpenMP DECLARE MAPPER and TILE
- Continue coarrays work for F08 feature complete
- Fortran quality and hardening, continuous perf improvements
- Auto-offload of Fortran DO CONCURRENT
- Fortran development: F18 C-interop, DLLIMPORT/EXPORT, /Qinit, /check:bounds

### Call to Action & Resources

### Call to Action – Get the Intel oneAPI Base, HPC & IoT Toolkit today!

• Current Customers - Log into Intel Registration Center - registrationcenter.intel.com

### Resources

- oneAPI Initiative <u>oneAPI.com</u>
- Intel<sup>®</sup> oneAPI Base Toolkit and HPC toolkit-<u>https://software.intel.com/content/www/us/en/develop/tools/oneapi/commercial-base-hpc.html</u>
- Intel<sup>®</sup> oneAPI Base and IoT toolkit
  - https://www.intel.com/content/www/us/en/developer/tools/oneapi/commercial-base- iot.html
- Porting Guide <u>https://software.intel.com/content/www/us/en/develop/articles/porting-guide-for-icc-users-to-dpcpp-or-icx.html</u>
- ICX OpenMP features support

https://www.intel.com/content/www/us/en/developer/articles/technical/openmp-features-and-extensions-supported-inicx.html

• IFX OpenMP features support

<u>https://www.intel.com/content/www/us/en/developer/articles/technical/fortran-language-and-openmp-features-in-</u> <u>ifx.html</u>

intel

# 

**OPENMP IN NVIDIA'S HPC COMPILERS** JEFF HAMMOND AND JEFF LARKIN 9 MAY 2022

# 

### **NVIDIA Compiler and Language Support**

Incremental Portable Optimization

### Accelerated Standard Languages

```
#pragma acc data copy(x,y) {
std::transform(par, x, x+n, y, y,
    [=](float x, float y){ return y + a^*x;
                                                  • • •
}
                                                  #pragma acc parallel loop
);
                                                  for (i=0; i<n; i++) {</pre>
                                                    y[i] += a * x[i];
                                                  }
                                                  • • •
do concurrent (i = 1:n)
  y(i) = y(i) + a*x(i)
enddo
                                                  #pragma omp target data map(x,y) {
                                                  • • •
                                                  #pragma omp target teams loop
import legate.numpy as np
                                                  for (i=0; i<n; i++) {</pre>
def saxpy(a, x, y):
                                                    y[i] += a * x[i];
   y[:] += a*x
                                                  }
                                                  • • •
```

Core Math	Communication Data Analytics
-----------	------------------------------

### Acceleration Libraries

https://developer.nvidia.com/nvidia-hpc-sdk-downloads

Platform Specialization

```
global
void saxpy(int n, float a,
           float *x, float *y) {
  int i = blockIdx.x*blockDim.x +
          threadIdx.x;
  if (i < n) y[i] += a*x[i];
int main(void) {
  • • •
 cudaMemcpy(d x, x, ...);
  cudaMemcpy(d y, y, ...);
  saxpy<<< (N+255) / 256, 256>>> (...);
  cudaMemcpy(y, d_y, ...);
   AI
                      Quantum
```



### **NVIDIA HPC COMPILER** Using OpenMP

- OpenMP
  - $\rightarrow$  Enable OpenMP targeting Multicore • -mp
  - $\rightarrow$  Enable OpenMP targeting GPU and Multicore -mp=gpu
- **GPU** Options
  - $\rightarrow$  Set GPU target, specialize for one generation, or many -gpu=ccXX
- **Compiler Diagnostics** 
  - -Minfo=mp  $\rightarrow$  Compiler diagnostics for OpenMP
- Environment variable for NOTIFY
  - export NVCOMPILER\_ACC\_NOTIFY = 1|2|3



# OPENMP MODEL

**OpenMP Execution Mapping to NVIDIA GPUs and Multicore** 

 $\rightarrow$  Starts Offload omp target

omp teams

omp parallel

simd omp

- [GPU] CUDA Thread Blocks in grid  $\rightarrow$
- $\rightarrow$  [CPU] num\_teams(1)
- [GPU] CUDA threads within thread block  $\rightarrow$  $\rightarrow$  [CPU] CPU threads
- [GPU] simdlen(1) i.e. ignored  $\rightarrow$  $\rightarrow$  [CPU] Hint for vector instructions

# WHY THE SUBSET?

# SCALABILITY-CHALLENGED OPENMP FEATURES

omp\_init\_lock() omp\_init\_lock\_with\_hint() omp\_set\_lock() omp\_test\_lock() omp\_unset\_lock() omp\_destroy\_lock() omp\_init\_nest\_lock() omp\_init\_nest\_lock\_with\_hint() omp\_set\_nest\_lock() omp\_test\_nest\_lock() omp\_unset\_nest\_lock() omp\_destroy\_nest\_lock()

MASTER SINGLE CRITICAL ORDERED SECTIONS BARRIER SIMD (SAFELEN) TASK TASKLOOP TASKGROUP DEPEND TASKWAIT CANCEL PROCBIND

Directives

Locks

https://developer.nvidia.com/gtc/2020/video/s21387

### Environment

OMP\_DYNAMIC OMP\_PROC\_BIND OMP PLACES OMP NESTED OMP WAIT POLICY OMP MAX ACTIVE LEVELS OMP THREAD LIMIT OMP CANCELLATION OMP\_DISPLAY\_ENV OMP\_MAX\_TASK\_PRIORITY

OMP SCHEDULE

OMP\_NUM\_THREADS

### START OFFLOADING 'OMP LOOP' Three Ways

### 1. omp target teams loop

- Recommended way
- You can use num\_teams and thread\_limit clauses
- 2. omp target loop
  - Fully automatic
  - You cannot use num\_teams / thread\_limit
- 3. omp target parallel loop
  - Uses only threads, and doesn't use teams
  - Might be useful for light kernels



### CASE STUDY: MATRIX TRANSPOSE OpenMP prescriptive parallelism

```
!$omp target teams distribute parallel do simd collapse(2)
do j=1,order
    do i=1,order
        B(i,j) = B(i,j) + A(j,i) ! Contiguous RW of B
    enddo
enddo
!$omp target teams distribute parallel do simd collapse(2)
do j=1,order
    do i=1,order
        B(j,i) = B(j,i) + A(i,j) ! Contiguous R of A
    enddo
enddo
```







# CASE STUDY: MATRIX TRANSPOSE

**OpenMP** descriptive parallelism

```
!$omp target teams loop collapse(2)
do j=1,order
 do i=1,order
   B(i,j) = B(i,j) + A(j,i)! Contiguous RW of B
 enddo
enddo
!$omp target teams loop collapse(2)
do j=1,order
 do i=1,order
   B(j,i) = B(j,i) + A(i,j) ! Contiguous R of A
 enddo
enddo
```

"teams loop" = more performance, less typing







# CASE STUDY: MATRIX TRANSPOSE Descriptive parallelism plus tiling

```
!$omp target teams loop collapse(2)
do jt=1,order,tile size
  do it=1,order,tile size
    !$omp loop collapse(2)
    do j=jt,min(order,jt+32-1)
      do i=it,min(order,it+32-1)
        B(i,j) = B(i,j) + A(j,i)! Contiguous RW of B
      enddo
    enddo
 enddo
enddo
!$acc parallel loop tile(32,32)
do j=1,order
 do i=1,order
    B(i,j) = B(i,j) + A(j,i)! Contiguous RW of B
 enddo
enddo
```

## 72% peak

### 76% peak





### CASE STUDY: AXPY Memory management options

allocate(X,Y,Z)	MAP_ALLOC	MANAGED	allocate	
X = 0	0	0	0.000015	•
Y = 0	1	1	0.348643	
$\mathbf{Z} = 0$	0	1	0.361456	
<pre>#if MAP_ALLOC !\$omp target data map(alloc:X,Y,Z) #else !\$omp target data map(tofrom: Z) &amp; !\$omp&amp; map(to: X,Y) #endif</pre>	1	0	0.000013	
<pre>! init do i=1,length X(i) = i-1 Y(i) = i-1 Z(i) = 0 enddo</pre>				

data in 2.367367 0.017112 0.018193 0.388539

init 0.014560 3.049976 3.055903 0.020914



# BEST PRACTICES FOR OPENMP ON GPUS

Use the teams and distribute directive to expose all available parallelism Use the **loop** directive when the mapping to hardware isn't obvious Aggressively collapse loops to increase available parallelism Use the target data directive and map clauses to reduce data movement between CPU and GPU ... or just skip the target data directive and use managed memory Use OpenMP tasks to go asynchronous and better utilize the whole system Use host fallback (if clause) to generate host and device code Use accelerated libraries whenever possible

Less is more with the NVIDIA compiler. Being pedantic can reduce performance.







### PANEL DISCUSSION

Moderator: Kalyan Kumaran (ANL) Panelists:

- Johannes Doerfert (LLVM, ANL)
- Carlo Bertolli (AMD)
- Tobias Burnus (GNU, Siemens)
- Deepak Eachempati (HPE)
- Xinmin Tian (Intel)
- Jeff Hammond (NVIDIA)







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### As of 4/15/2021 **MULTIPLE COMPILERS WILL SUPPORT A COMMON SET** OF OPENMP DIRECTIVES ON GPUS (NON-EXHAUSTIVE LIST) (1/2)

	LLVM/Clang	AMD	HPE/Cray	IBM	Intel	NVIDIA	GNU
Levels of parallelism	2 (teams + parallel), eventually SIMD	2 (teams, parallel)	2 (teams, parallel or simd)	2 (teams, parallel)	3 (teams, parallel, simd)	2 (teams, parallel)	3 (teams, parallel, simd)
OpenMP directive							
target	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$
declare target	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$
map	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$
target data	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$
target enter/exit data	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$
target update	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$
teams	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$
distribute	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$
parallel	$\checkmark$	$\checkmark$	$\checkmark$ (may be inactive)	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$
for/do	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$
reduction	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$
simd	<ul> <li>✓ (used for optimization, not for mapping)</li> </ul>	√ (on host)	$\checkmark$	√ (ignored)	$\checkmark$	√ (ignored)	$\checkmark$
atomic	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$
critical	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	X	$\checkmark$
sections	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	X	$\checkmark$
master	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$
single	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$
barrier	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$
	V	$\checkmark$	√ (C/C++ partial)	×	$\checkmark$	X (planned)	√ (C/C++) <b>X</b> (OG11)
Managed by Ocinicago Argor	ine, LLC.						

### MULTIPLE COMPILERS WILL SUPPORT A COMMON SET OF OPENMP DIRECTIVES ON GPUS (NON-EXHAUSTIVE LIST) (2/2)

			-				
	LLVM/Clang	AMD	HPE/Cray	IBM	Intel	NVIDIA	GNU
loop directive	eventually	×	$\checkmark$ (Fortran only)	×	$\checkmark$	$\checkmark$	<b>X</b> (OG12)
collapse of a perfectly nested loop	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$
collapse of an imperfectly nested loop	$\checkmark$	√ (c/c++)	$\checkmark$	×	X	X	X (OG12)
collapse of a non-rectangular nested loop	$\checkmark$	√ (c/c++)	$\checkmark$	×	$\checkmark$	X	$\checkmark$
array reduction	$\checkmark$	X	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	X (OG12)
requires unified_shared_memory	$\checkmark$	X	X (WIP CCE 13)	$\checkmark$	$\checkmark$	X (planned)	X (OG11)
requires dynamic_allocators	eventually	X	X	X	$\checkmark$	X	X (OG11)
declare reduction	eventually	$\checkmark$	$\sqrt{(C/C++ only)}$	$\checkmark$	√ (for C++) X (for Fortran)	×	$\checkmark$
declare mapper	$\checkmark$	X	X (WIP CCE 13)	X	X (WIP)	X	<b>X</b> (OG12)
metadirective	LLVM 13	X	√ (Fortran only)	X	X (WIP)	X (planned)	X (OG12)
"target nowait" supporting asynchronous execution	$\checkmark$	X	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$
"target depend" supporting fine-grained dependencies	$\checkmark$	X	$\checkmark$	$\checkmark$	$\checkmark$	X (planned)	$\checkmark$
"target device" supporting multiple non-host devices per process	$\checkmark$	X	X (WIP CCE 13)	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$
use_device_addr	$\checkmark$	$\checkmark$	$\checkmark$	×	$\checkmark$	$\checkmark$	$\checkmark$
detachable tasks: "detach" clause and "omp_fulfill_event" runtime routine	$\checkmark$	$\checkmark$	$\checkmark$	×	X	X	$\checkmark$
Memory management APIs							
allocate directive for allocating variables in managed memory via allocator	$\checkmark$	X	✓ (extension)	×	$\checkmark$	X	X (OG11)
allocate clause for allocating privatized variables in managed memory via allocator	$\checkmark$	X	$\checkmark$ (extension)	X	$\checkmark$	X	<b>X</b> (OG11)
APIs for allocating/freeing memory via allocator	$\checkmark$	X	$\checkmark$	×	$\checkmark$	X	$\checkmark$
APIs for defining new allocators with custom traits (e.g. pinned memory)	$\checkmark$ (not fully implemented)	×	$\checkmark$	X	$\checkmark$	×	🗶 (OG11)
Interop objects and APIs	$\checkmark$	×	X (planned CCE 13)	×	X (WIP)	×	X (OG12)